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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/617,441	07/14/2000	HIROTAKA KAWATA	106310	5358

25944 7590 08/20/2003

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EXAMINER	
BROCK II, PAUL E	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 08/20/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Offic Action Summary	Application No.	Applicant(s)	
	09/617,441	KAWATA, HIROTAKA	
	Examiner	Art Unit	
	Paul E Brock II	2815	

-- The MAILING DATE of this communication appears n the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 June 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8,20,21 and 24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8,20,21 and 24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 July 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on ~~*20 August 2002*~~ 7/26/02 is: a)☒ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *24* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 3 – 7, and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Nakazawa et al. (USPAT 5614730, Nakazawa).

With regard to claim 1, Nakazawa discloses in figures 19a – 19c and 20 an electro-optical device. Nakazawa discloses in figures 19a – 19c and 20 a substrate (109). Nakazawa discloses in figures 19a – 19c and 20 a pixel electrode. Nakazawa discloses in figures 19a – 19c and 20 a scanning line (101). Nakazawa discloses in figures 19a – 19c and 20 a data line (108) crossing the scanning line. Nakazawa discloses in figures 19a – 19c and 20 a transistor disposed correspondingly to an intersection between the data line and the scanning line. Nakazawa discloses in figures 19a – 19c and 20 the transistor including a gate electrode (103). Nakazawa discloses in figures 19a – 19c and 20 a semiconductor (102) layer, wherein the semiconductor layer comprises a source region (enlarged part of the semiconductor layer to the right of the gate electrode) that is connected to the pixel electrode through a contact hole (1905), a drain region (enlarged part of the semiconductor region to the left of the gate electrode) that is connected to the data line through a second contact hole (1906), a channel region (portion of 102 directly under gate electrode) disposed under the gate electrode, and a semiconductor portion (portion

between 103 and 1905) protruding out of the channel region and not being covered with the gate electrode.

With regard to claim 3, Nakazawa discloses in column 4, lines 3 – 12 the semiconductor region forming the transistor comprises polycrystalline silicon.

With regard to claim 4, Nakazawa discloses in column 3, line 57 the substrate being an insulative substance.

With regard to claim 5, Nakazawa discloses in column 3, line 57 the substrate being an quartz substrate.

With regard to claim 6, Nakazawa discloses in column 3, line 57 the substrate being an glass substrate.

With regard to claim 7, Nakazawa discloses in figure 23b a second substrate (313) disposed opposing a surface of the first substrate. Nakazawa discloses in figure 23b liquid crystals (312) sandwiched by the first substrate and the second substrate, and driven by transistor elements formed on the semiconductor layers.

With regard to claim 20, as far as the examiner can ascertain, Nakazawa discloses in figures 19a – 19c and 20 the semiconductor portions protrudes in a direction in which the scanning line extends.

With regard to claim 24, Nakazawa discloses in figures 19a – 19c and 20 an electro-optical device. Nakazawa discloses in figures 19a – 19c and 20 a substrate (109). Nakazawa discloses in figures 19a – 19c and 20 a plurality of pixel electrodes. Nakazawa discloses in figures 19a – 19c and 20 a plurality of scanning lines (101). Nakazawa discloses in figures 19a – 19c and 20 a plurality of data lines (108)one of the data lines crossing one of the plurality of

scanning lines. Nakazawa discloses in figures 19a – 19c and 20 a plurality of transistors disposed correspondingly to intersections between the plurality of data lines and the plurality of scanning lines. Nakazawa discloses in figures 19a – 19c and 20 each of the plurality of transistors including a gate electrode (103) and a semiconductor layer. Nakazawa discloses in figures 19a – 19c and 20 a semiconductor (102) layer, wherein the semiconductor layer comprises a source region (enlarged part of the semiconductor layer to the right of the gate electrode) that is connected to one of the plurality of pixel electrodes through a contact hole (1905), a drain region (enlarged part of the semiconductor region to the left of the gate electrode) that is connected to one of the plurality of data lines through a second contact hole (1906), a channel region (portion of 102 directly under gate electrode) disposed under the gate electrode, and a semiconductor portion (portion between 103 and 1905) protruding out of the channel region and not being covered with the gate electrode.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nakazawa as applied to claim 1 above, and further in view of Watanabe et al. (USPAT 5316960, Watanabe).

Nakazawa does not disclose the semiconductor region forming the transistor comprises monocrystalline silicon. Watanabe teaches in column 4, lines 22 – 26 that monocrystalline silicon is a well known material with which to form a semiconductor region. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use monocrystalline silicon of Watanabe as the semiconductor for the transistor of Nakazawa in order to select a layer with desired channel characteristics.

5. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nakazawa as applied to claim 1 above, and further in view of one of ordinary skill in the art.

It has been held in In re Pearson 181 USPQ 641 (CCPA) that intended use does not avoid prior art. Therefore, it would have been obvious to use the device of claim 1 as an LCD projector.

6. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nakazawa as applied to claim 1 above, and further in view of Nishihara et al. (JPPAT 06163891, Nishihara).

Nakazawa discloses in figures 19a – 19c and 20 wherein the gate electrode has two parts protruding out of the semiconductor layer. Nakazawa does not teach that the source or drain region is disposed between the two parts of the gate electrode protruding out of the semiconductor layer. Nishihara teaches in figures 3 and 4 a gate electrode (11) having two parts (part below a semiconductor layer, and the part to the above left of the semiconductor layer) protruding out of a semiconductor layer, and the drain (14a) being disposed between the two parts. It would have been obvious to one of ordinary skill in the art at the time of the present

invention to use the two parts of the gate electrodes of Nishihara in the device of Nakazawa in order to reduce the mounting area as stated in the abstract of Nishihara.

Response to Arguments

7. Applicant's arguments filed June 11, 2003 have been fully considered but they are not persuasive.

8. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., "a semiconductor portion that protrudes out of the gate electrode") are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). Therefore, the applicant's arguments are not persuasive, and the rejection is proper.

9. With regard to the applicant's argument that "the semiconductor layer 102 [of Nakazawa] is only shown disposed between the first part (source) and the second part (drain), and not 'protruding out of the channel region and not being covered with the gate electrode'," it should be noted that Nakazawa does teach all three of these portions. As shown in figure 19a of Nakazawa a semiconductor region that protrudes outside of the channel region and not covered by the gate electrode can be found between the gate electrode and either of the drain contact or

the source contact. Therefore, the applicant's arguments are not persuasive, and the rejection is proper.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul E Brock II whose telephone number is (703)308-6236. The examiner can normally be reached on 8:30 AM-5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (703)308-1690. The fax phone numbers for the organization where this application or proceeding is assigned are (703)308-7722 for regular communications and (703)308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

Paul E Brock II
August 18, 2003